

Appl. No. 10/815,201

Attorney Docket No.: N1280-00180 (TSMC2003-1083)

Reply dated: 11/01/05

Response to Office Action of: 07/01/2005

**Amendments to the Specification:**

Please amend paragraph [0024] of the specification according to the following amended paragraph:

During the high temperature alloy process, not only does the metal diffuse into the silicon layers; but also, the silicon diffuses into the deposited metal layer, from both the single crystal silicon island 202 and the connecting poly layer 210. Metal-silicide is therefore formed in a continuous layer 232, even across the narrow gate oxide layer edge 230. Continuous layer 232 thereby bridges the gap formed by the edge of gate oxide 212, between single crystal silicon island 202 and connecting poly layer 210.

Continuous layer 232 is formed by respective lateral encroachment of a silicide film formed of the silicidation of the metal layer and single crystal silicon island 202 and a silicide film formed of the silicidation of metal layer 202 and connecting poly layer 210. Continuous layer 232 thereby consists of a first silicide film that includes silicon from single crystal silicon island 202 and a second silicide film that includes silicon from connecting poly layer 210. As such, the gate oxide 212 no longer separates the silicon island 202 from the connecting poly silicon layer 210. This continuous silicide layer 232 is said to have a sidewall butted connection structure. From the perspective of an SRAM cell, this metal-silicide layer may serve as a local intra-cell connection mechanism between the pull-up P-channel metal-oxide-semiconductor field effect transistor (PMOSFET) and the pull-down NMOSFET, wherein the SOI P-active area is directly and continuously connected with the SOI N-active area.